COINCIDENT CURRENT MAGNETIC CORE MEMORIES

by

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INTRODUCTION

The stored program digital computer brought about a need for a large random access digital memory. Early computers used a rotating magnetic drum. This had the disadvantage that when a particular piece of information was needed, the machine had to wait while the drum rotated to the correct position. Magnetic core memories have alleviated this difficulty. Core memories can store or retrieve any desired piece of information in a fixed short cycle time regardless of its location.

The coincident current magnetic core memory has been in use for over ten years. In this time, much research has been done on a variety of new techniques. Many of these show promise of higher speeds and larger capacities than can be attained using coincident current core memories. However, none has replaced the core memory in practical use. Only in a few large high speed applications have other techniques been used at all for a practical computer.

Meanwhile, continuing engineering improvements have made the coincident current core memory capable of ever increasing speeds and capacities. It is doubtful that this type of memory will ever be completely replaced. It will probably continue to be the most widely used for many years.

CHAPTER I

CORE PROPERTIES

The magnetic core as used in digital memories is described by Quartly (1) as a toroid shaped piece of ferrite with a composition MFe_2O_4, where M is some divalent metal such as magnesium or manganese. This type of ferrite has a very low conductivity, on the order of 10^{-5} mho-cm, which means it has very small eddy current losses when placed in a varying magnetic field.

Ferrites also have a nearly rectangular hysteresis loop or B-H curve similar to the one shown in Fig. 1. This characteristic will be discussed later. Some early cores were made of an iron alloy with suitable B-H characteristics, rolled into a very thin tape to reduce eddy current losses, and wound around a ceramic bobbin. Such cores have not come into extensive use because of several disadvantages, including higher cost and slower operation.

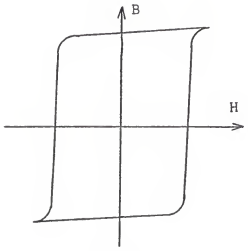

Figure 1

A Typical B-H Characteristic for a Ferrite Core.

The B-H characteristic in Fig. 1 relates magnetic flux density B inside the material to magnetic field intensity H. In the case of toroid cores, the direction of both B and H, which are in general vector quantities, will be assumed always to be tangent to a circle within the core and concentric with it as shown in Fig. 2. Furthermore, both B and H will be assumed to be of constant magnitude throughout the core. These assumptions actually represent appropriate averages over the interior of the core, but they are adequate to describe the external properties of the core as utilized in digital memories. A more complete description of the internal magnetic behavior of the core involves a detailed study of heterogeneous effects within the material. Such a study is beyond the scope of this paper, and such effects will be discussed only superficially in passing. For more detailed information, see Wang (2).

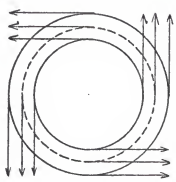

Figure 2

Assumed Direction of B and H in a Core.

A ferromagnetic material is characterized by small internal regions called domains which are magnetically saturated. This means that all atoms have their magnetic moments aligned in the same direction, giving rise to a total magnetic moment for the domain. An unmagnetized material has its domains oriented at random so that the net magnetization of the material is

zero. Fig. 3a shows a simplified model of such a material with four equal sized domains arranged so that their magnetic moments cancel.

When an external magnetic field is applied, the domains tend to rearrange themselves in such a way that the net magnetic moment over all domains is non-zero and is aligned in the direction of the applied field. This occurs through two separate mechanisms, domain growth and rotation of domain magnetization.

Domain growth is represented by the simplified model in Fig. 3b. The domains which are oriented in the direction of the applied field grow at the expense of those which are oriented in less favorable directions. This is accomplished when atoms on the boundary of the shrinking domain realign themselves with the growing domain.

Analysis shows that a domain boundary is actually a wall of finite thickness rather than an abrupt line. Associated with it is an energy which is a complicated function of its position. As long as the wall does not move beyond a monotonic region of this energy function, the process is reversible. That is, if the applied field is removed, the domain wall will return to its original position. When the wall moves past a local maximum of the energy function, the process becomes irreversible, and the wall will not return to its original position when the external field is removed.

Rotation of domain magnetization is represented by the simplified model in Fig. 3c. A magnetic domain is characterized by an "easy axis" or a direction of magnetization determined by the crystal structure along which the energy due to its magnetization is at a minimum. When no external field exists, the magnetic moment of the domain will lie along this easy axis. An applied external field will cause the domain magnetic moment to rotate from the easy axis to some direction between the easy axis and that of the applied

field. This process is reversible.

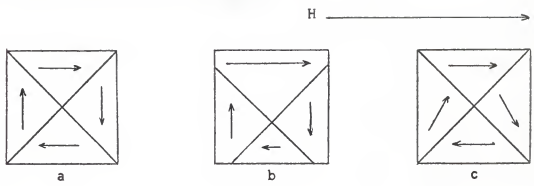

Figure 3

A Model of the Domains in a Core.

Now let us examine the external behavior of a core in the light of all this. The field intensity H is that of the externally applied circular magnetic field, while the flux density B is that arising from the sum of the externally applied field and the net internal circular magnetization over all domains. Consider the B-H curve of Fig. 4 and assume that the core is magnetized so that the flux density is $-B_r$, with no external field applied. This corresponds to the point A in Fig. 4. If the external field is increased slowly to the value H_m, the core follows the curve in the direction of the arrows to point C.

Under weak fields, the principle effect is reversible domain growth with a very small amount of irreversible domain growth. As the field intensity increases, irreversible growth becomes more and more important. Near saturation, the major effect is rotation. The figure indicates these regions.

Now if H is reduced to zero, the core will return to point D, because only the reversible magnetization changes will revert to their original state. Decreasing H to $-H_m$ and increasing it to zero again returns the core to point

A. The ability of the core to retain information arises from the fact that it can be left at either point A or point D with no external field.

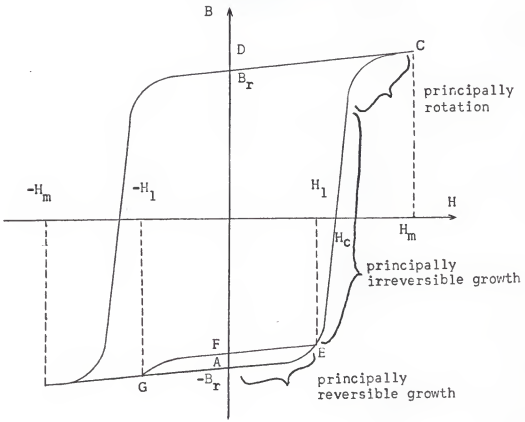

Figure 4

Flux Changes in a Core.

If H is varied in smaller increments, minor loops are described. For example, if H is increased to H_1, the core moves to point E with only a small amount of irreversible magnetization occurring. Now when H is reduced to zero, the core will move to point F. Decreasing H to $-H_1$ and increasing it to zero several times will result in a stable loop G-E as shown. The appropriate sequence of values of H will establish minor loops anywhere

within the outermost loop.

In this paper the group of states near state A in Fig. 4 and the group near state B will be called major states while each individual state will be called a minor state. For example, in Fig. 4 the points A, E, F, and G all belong to the same major state but are different minor states.

For a particular core geometry, the field intensity H is proportional to the magnetomotive force which is equal to the current I linking the core. Also for a particular geometry, the flux density B is proportional to the flux ϕ. Thus, for a specific core the B-H characteristic can be drawn with the axes calibrated in terms of ϕ and I rather than B and H.

CHAPTER II

THE COINCIDENT CURRENT MEMORY

The coincident current memory takes advantage of the B-H characteristics of the ferrite core both to store digital information and to simplify address decoding.

A digital memory is organized in groups of bits called words, which are always accessed together. Each word is numbered, its number being called its address. A memory cycle involves either obtaining from the memory the data in a word and putting it into a register, or putting the data in a register into a word in the memory. In either case, the address of the word to be read or written must be specified. In the case of writing into the memory, the previous data in the addressed word is destroyed, and the new data from the register replaces it. Reading from the memory, on the other hand, must be done non-destructively--that is, so that the data in the word is not destroyed and may be read again later.

This is found to be a rather difficult task. One type of memory which actually reads non-destructively will be discussed later. For the present, we shall be satisfied with a process which resets the contents of the word to all 0's during reading. Later in the cycle the original data can be rewritten into the addressed word. This is logically equivalent to non-destructive read-out. This process has the further limitation that it cannot simultaneously write 0's in some bit positions of the addressed word and 1's in others. Instead, the word must first be reset to all 0's, and then 1's can be written

into the appropriate bit positions. Because of all this, a combined cycle involving a read operation first, then a write operation will be used for both logical reading and logical writing. This cycle differs little in which type of logical operation it is to perform.

Fig. 5 shows a small array of cores in a plane, wired for use in a coincident current memory. Each core is threaded by four wires. Along each row is one X drive wire, and along each column is one Y drive wire. There are two wires threading every core in the plane. The inhibit, or digit wire, runs back and forth vertically. The sense wire runs along diagonal lines for reasons which will be discussed later. The reference directions of the

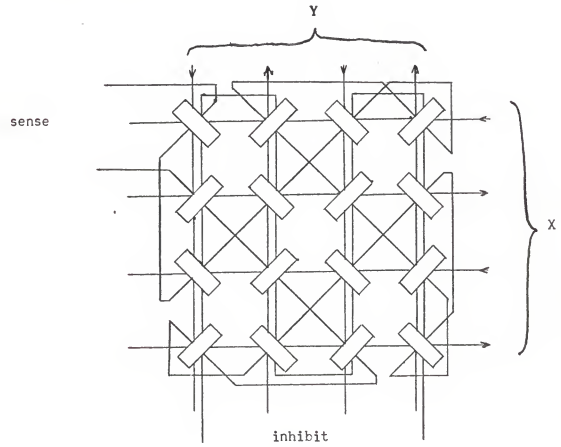

Figure 5

Memory Plane Wiring.

X and Y drive wires alternate as shown by the arrows. One plane has as many cores as there are words, and there must be a separate plane for each bit of a word.

Fig. 6 shows the way in which several planes are interconnected to make a complete storage array. A single drive wire of one plane is connected in series with the corresponding drive wires in all other planes. The inhibit and sense wires of each plane are separate.

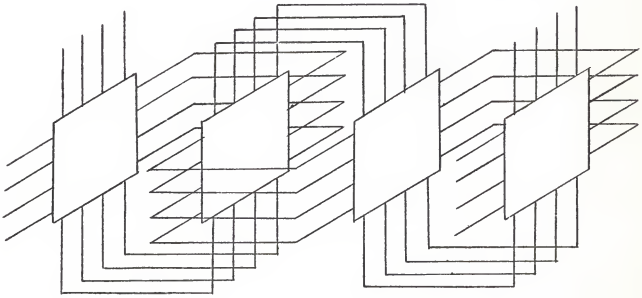

Figure 6

Interconnection of Memory Planes.

Now consider Fig. 7. Any core at point A is considered to contain a 1, and any core at point B is considered to contain a 0. Suppose a current pulse of $-\frac{I_m}{2}$ is caused to flow through one X drive wire. This is called half read select current. Each core on the selected wire will move to point C or D depending on its original state, and then return approximately to point A or B when the current falls, describing a minor loop.

Now suppose such a pulse is applied to one X and one Y drive wire simultaneously. Each core on either wire will behave as described before except the one at the point where the two selected wires intersect. This core is linked by a current of $-I_m$ and will be driven to point E, regardless of its previous state. If it previously contained a 1, the changing flux ϕ linking the wires threading the core will induce a voltage on them. In particular, the sense wire will be used to detect this voltage pulse. If the core contained a 0, the voltage across the sense winding will be less, due to the smaller flux change.

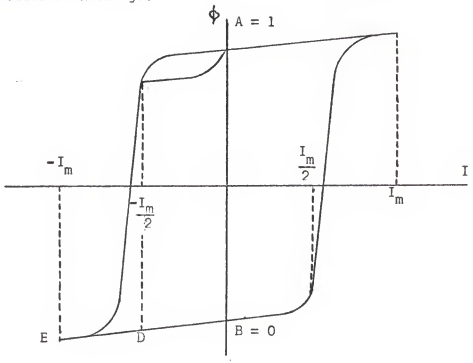

Figure 7

States of a Core in the Memory.

In each plane, only the core at the intersection point of the selected X and Y drive wires has now been switched. Those on only one of the selected wires have been disturbed but have not changed their major states. Those which lie on neither the selected X wire nor the selected Y wire will be

undisturbed. Thus, one word consisting of one bit from each plane has been set to all 0's, and its former contents have been available at the sense wires as a set of pulses usable for setting the latches of a register.

Now the word can be rewritten into the selected cores. A current pulse of $+\frac{I_m}{2}$ is now delivered to the selected drive wires. This is called half write select current. In addition, a current $-\frac{I_m}{2}$ is caused to flow in the inhibit winding of every plane where a 0 is to be written. Let us now consider the current linking the cores in different positions in the array.

All cores on neither selected drive wire and in a plane where a 1 is to be written are undisturbed. All cores on neither selected drive wire but in a plane where a 0 is to be written are linked by $-\frac{I_m}{2}$ flowing in the inhibit wire and describe minor loops. All cores on only one selected drive wire in a plane where a 1 is to be written are linked by $\frac{I_m}{2}$ flowing in the drive wire and describe minor loops in the positive direction. Those on one selected drive wire in a plane where a 0 is to be written are linked by $\frac{I_m}{2}$ in the inhibit wire, totalling zero. These cores will describe minor loops in the negative direction, however, because the inhibit current pulse usually begins earlier and ends later than the drive current pulses. At the intersections of the selected drive wires and in planes where a 1 is to be written, cores are linked by $\frac{I_m}{2}$ flowing in each drive wire totalling I_m and are thus set to 1. Those at the intersections of the selected drive wires in planes where a 0 is to be written are linked first by $-\frac{I_m}{2}$ flowing in the inhibit wire, and then by $+\frac{I_m}{2}$ when the drive currents rise, and again by $-\frac{I_m}{2}$ when the drive currents fall before the inhibit current falls. Thus these cores describe a minor loop to either side of the Φ axis.

In all these cases, only the cores where the drive wires intersect and in planes where a 1 is to be written are switched. Where a 0 is to be written,

the cores are actually not switched. They were switched to 0 during the read portion of the cycle and are merely left there during the write portion.

If a logical read operation is to be performed, the word written during the write portion of the cycle is merely that read during the read portion. If a logical write is to be performed, the word read during the read portion is discarded and the word to be written is obtained from some other source.

CHAPTER III

THE NOISE PROBLEM

Now let us examine more carefully the behavior of a partially selected core and the minor loops it describes during these operations. These are presented in detail by McNamara (3). We shall be concerned with "read disturbing," that is driving the core with half read select current $-\frac{I_m}{2}$ and "write disturbing," that is driving it with half write select current $+\frac{I_m}{2}$.

After a read drive, any core of the selected word is at point B in Fig. 8. A write 0 operation moves the core to point C as inhibit current rises, back to point D as select currents rise, and through E and F to G as first select and then inhibit currents fall. If the core is read as would occur in a half read select or half write select with inhibit sequence, it moves over the minor loop F-G. The state G is described as reversible (with respect to read disturbing only) because the core returns to it when the disturbing current falls.

If the core is write disturbed, as would occur if it received half write select current without inhibit current, it moves through point H to point I. This is described as an irreversible state (again only with respect to a read operation) because a half read select current pulse causes the core to return to a different state, namely K, at the end of the pulse. Hereafter, a stable loop is formed; a read disturb sequence always moves the core through state J to state K and a write disturb sequence always moves it through state H to state I.

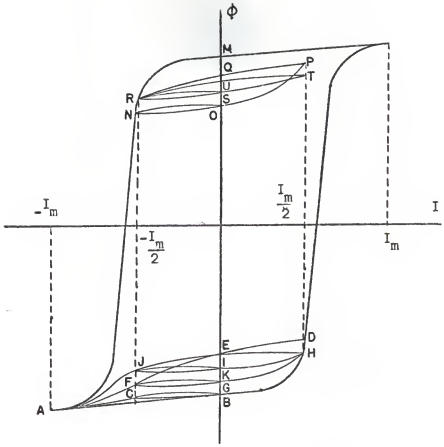

Figure 8

Minor Loops Caused by Half Selecting.

Similarly, after a 1 is written, the core is in state M. When the core is first read disturbed it moves through N to O. Repeated read disturbing causes it to move around the minor loop N-O. When it is write disturbed, it moves through P to Q. Hereafter, a stable loop is formed and read disturbing always moves the core through state R to state S. Write disturbing always moves it through state T to state U. Repeated read disturbing moves it around minor loop R-S. Notice that state U is an irreversible state and state S is a reversible state, both with respect to half read signals.

These minor hysteresis loops and their slightly different states for cores containing 1's or 0's give rise to serious noise problems in sensing a selected core. The voltage pulses induced in the sense winding due to reversible changes are relatively short as shown in Fig. 9. Those induced by irreversible changes are longer. In a memory plane all cores that are half selected as well as the one which is selected contribute to the sense voltage. Frequently, because of the large number of half selected cores, the sense wire noise due to their irreversible switching exceeds the wanted signal voltage due to the irreversible switching of the selected core. Also, because of the speed of the reversible changes, the first peak of the sense voltage which they cause may be higher than that due to the switching of the selected core despite its considerably larger flux change. This is the reason that the diagonal sense wiring geometry is used.

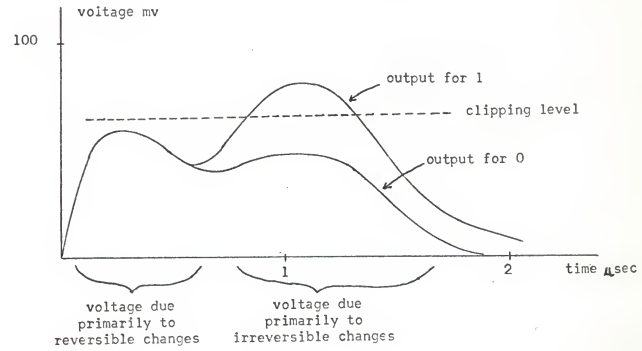

Figure 9

Sense Voltage Output During Reading.

This geometry is shown in Fig. 10, with the inhibit wire omitted for clarity. Arrows are drawn to show the reference directions of the drive and sense wires at each core. The sense wire is arranged so that it links half the cores in one direction and half in the other with respect to their defined direction of magnetization (defined by the directions of the drive wires threading them). In an n x n plane along any drive wire, there are $\frac{n}{2}$ cancelling pairs of cores. When the core at the intersection of two drive wires is removed from consideration as a half selected core, one pair is disrupted from each wire, leaving $\frac{n}{2}$-1 cancelling pairs on each wire or n-2 altogether and two uncancelled cores.

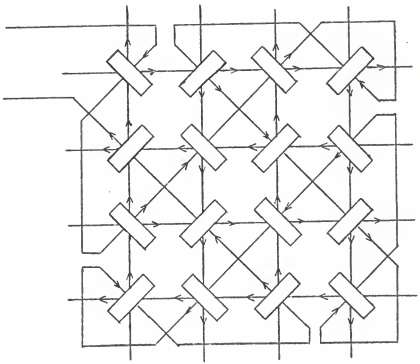

Figure 10

Cancelling Sense Winding Geometry.

The two cores of a pair do not actually cancel perfectly, because the noise voltages developed by each are not necessarily equal. Differences in the major or minor states of the two cores and differences in the core properties themselves can lead to imperfect cancellation. A particular type of core has a delta noise voltage V_δ defined by Womack (4) as the average voltage difference in half select outputs due to imperfect cancelling between cores. For an n x n plane, there will be a delta noise voltage (n-2) V_δ developed across the sense winding.

The two uncancelled cores have a "half select noise voltage" V_h defined as the maximum voltage induced by the core when half selected. This gives rise to an additional voltage of $2V_h$ at the sense winding terminals. The total noise voltage is $2V_h + (n-2)V_\delta$.

A third type of noise called digit plane noise exists on the sense wire at times other than reading time (5). When a drive line is excited, the capacitive coupling to the sense winding causes a large common mode noise voltage to appear at both sense winding terminals. This is not serious in itself, as only the voltage across the sense winding terminals is of interest. However, this common mode voltage also leads to a sustained ringing difference across the sense winding. This is caused by 1) coupling of common mode noise between various parts of the sense winding along the unselected drive wires, and 2) the fact that a point on the sense wire where common mode noise is generated is in general at unequal distances from the two ends of the line.

This voltage does not appear at read time and it would be unimportant except that it delays the completion of a memory cycle. Furthermore, it is of such magnitude that it will saturate a sense amplifier which is designed

to detect the smaller signals present during read time. Additional delay is involved while the amplifier recovers.

The time elapsing between 10% and 90% of the flux change is defined by Quartly (1) as the core switching time T. It is given by $T=\frac{S}{H-H_o}$ where H is the applied field, H_o is a value of field intensity approximately equal to H_c in Fig. 4, and S is a "switching coefficient" for the material. Since the ratio of $H = H_m$, as will be used, to H_o is constant, cores with large values of H_o will switch faster. To do this, it becomes necessary to reduce the path length around the core if the required drive currents are not to become excessive. Thus faster switching cores must be made smaller.

Because of the cancelling sense winding geometry, the wanted sense voltage output for a core in its 1 state may be of either sign. Therefore, the sense amplifier which discriminates between 1 and 0 outputs must accept a signal of either polarity and eventually rectify it. Since the signal is at very low amplitude, and since rectifying devices have some sort of threshhold voltage associated with them which is of magnitude similar to that of the signal, it is necessary to amplify the signal first with some sort of bipolar amplifier. Furthermore, because the sense amplifier may receive an extended sequence of pulses of the same polarity, it must be immune to DC level shift.

The simplest means of discriminating between a 1 and a 0 output is clipping the signal and passing only that portion which exceeds a set voltage. This technique is effective only if the noise voltage is enough less than the 1 output voltage to establish a clipping level with adequate margin for changes in operating conditions. Fig. 9 shows a typical sense winding voltage and a clipping level used to determine the state of the selected core.

An additional sensing technique uses strobing of the sense amplifier so that the early part of the sense voltage is ignored. Fig. 11 shows a typical sense winding voltage. Between time t_1 and t_2, the sense amplifier is strobed or enabled, so that it accepts a signal only during this interval. The component of voltage due to reversible changes has reached a small value by time t_1 and does not present so serious a problem in establishing a clipping level.

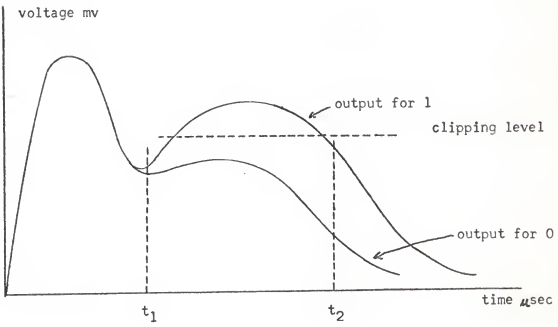

Figure 11

Clipping and Strobing the Sense Voltage.

A technique called noise matched clipping has been developed by Tsui (6) for improvement in sensing large arrays with their larger noise voltages. Fig. 12 shows a sense winding voltage as the sum of a noise signal and a wanted signal. The noise voltage decreases in a fashion approximating an

exponential decay. The noise matched clipping technique generates an exponentially decaying voltage somewhat above the maximum noise voltage for a zero output and uses this as a time varying clipping reference level. Thus a larger portion of the wanted signal is available to the sense amplifier. Theoretically, if a clipping level can be established and maintained at all, then discriminating between 1 and 0 outputs is no problem. However, in very large, high speed memories, with critical design problems, the additional signal energy available is of considerable value.

Tsui also found that it is desirable to strobe the first stage of the sense amplifier. Because this stage must be bi-polar, strobing on early amplifiers was often done at a later stage, after rectification, affording a circuit simplification. However, the first stage strobing technique can be used to prevent the amplifier from saturating when subjected to the digit plane noise.

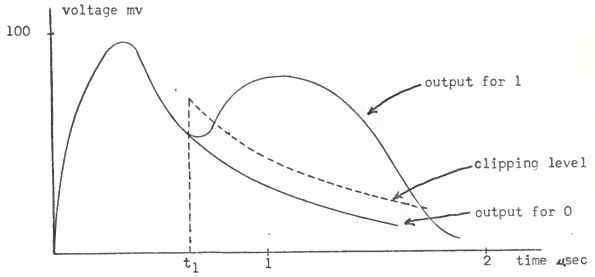

Figure 12

Noise Matched Clipping.

An early vacuum tube memory had difficulties with serious variations in both the time of rise and the wave form of the drive currents because of its large physical size and many drive circuits. This made it difficult to time the sense amplifier strobe signal properly. This was solved by returning all X and Y drive currents through a common wire (Fig. 13). A separate core on this wire provided a signal to a single sense amplifier whose output was used to time the strobe pulse. Since no other cores drove this sense amplifier, no delta noise or half-select noise was present, and the resulting signal indicated very closely when the selected memory core was switching, despite irregularities in drive currents.

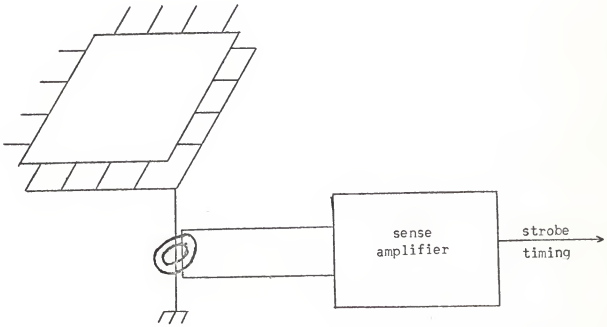

Figure 13

Strobe Signal Timing.

Womack (4) has developed a worst case method which he calls "Schmoo Plot Analysis" for evaluating the performance and requirements of a core array. Fig. 14a shows a typical ϕ-I characteristic for a core. I_b is a value close to the knee of the characteristic. It is not to be exceeded by the half select current if minor loops are to be kept small. If the core is to be completely switched, however, the half select current must be at least $\frac{I_m}{2}$. A plot of write half select current I_w versus read half select current I_r is shown in Fig. 14b. Both these currents must lie in magnitude between $\frac{I_m}{2}$ and

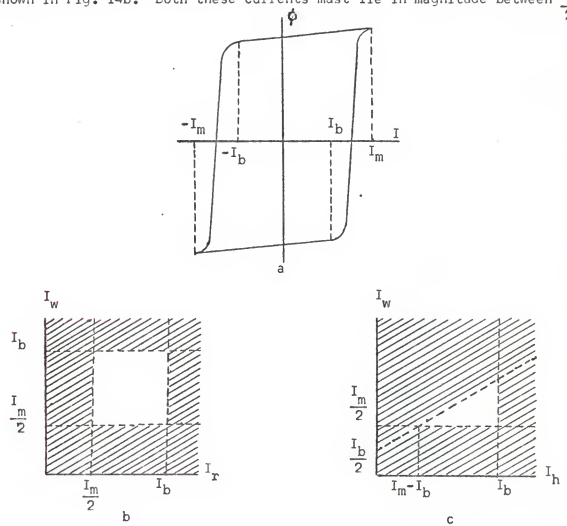

Figure 14

Allowable Operating Conditions.

I_b for correct operation. These maximum and minimum values are shown on the plot and the unshaded area is that where all requirements are met.

Fig. 14c shows a plot of I_w versus inhibit current I_h. I_h cannot exceed I_b, or completely unselected cores containing 1's in a plane where a write zero operation is performed will be partially reset toward the zero state. As before, I_w must be at least $\frac{I_m}{2}$. These restrictions are indicated on the plot. Furthermore, the full write select current $2I_w$ minus the inhibit current must not exceed I_b or cores where 0's are to be written will be partially set toward the 1 state. This requirement can be written $2I_w - I_h \leq I_b$ or $I_w - \frac{I_h}{2} \leq \frac{I_b}{2}$. This restriction is indicated by the diagonal line on the plot. Any point within the unshaded area satisfies these three requirements.

When I_w, I_r, and I_h are all plotted in a three dimensional graph, the restrictions imposed on them result in a wedge shaped figure containing the points of successful operation as shown in Fig. 15a. When noise voltage is taken into account, the region of successful operation shrinks somewhat into an irregular shape which has been called a schmoo. This is shown in Fig. 15b. Various cross sections of the schmoo are called schmoo plots.

A machine to display schmoo plots for an actual array was built by Womack. The array is repeatedly accessed with one of the various currents held fixed and the other two varied over suitable ranges in small steps between cycles. One of the two varying currents is held at one level while the second reaches the end of its range. These two currents are used as X and Y deflection signals to a cathode ray oscilloscope resulting in a systematic scan of the entire screen. The beam is blanked whenever an error free operation is performed. The result is a plot like that in Fig. 15c with the blank

area representing a cross section of the schmoo. These plots give actual experimental worst case data on a particular memory array showing allowable values of the drive currents to be used with the array. Notice that the limiting values of one particular current are not fixed but depend on the values of the others.

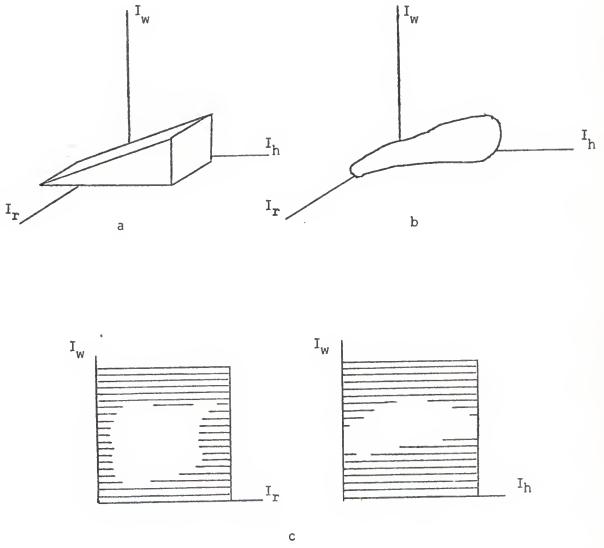

Figure 15

Schmoos and Schmoo Plots.

CHAPTER IV

IMPROVEMENTS AND SOLUTIONS TO PROBLEMS

A number of improvements to the coincident current memory have been suggested and tried. When memories are to be made larger and faster, the problems worsen, and without some additional techniques become insurmountable.

A larger plane means more half selected cores and more delta noise. One of the simplest means of reducing it is to divide the sense winding into several parts, each with its own sense amplifier. This increases the maximum plane size obtainable but requires more sense amplifiers. It also requires gating circuits to select the correct sense amplifier output.

Another technique is to stagger the rise of the X and Y drive currents. If the X drive current rises first, the Y drive current can be delayed until the delta noise signal due to the X line half selected cores has decayed. Then when the Y drive current rises, the resulting noise on the sense wire is due to half selected cores on the Y line only. This of course slows the operation of the memory. Furthermore, the plane can be made non-square so that there are many more X half selected cores than Y half selected cores, resulting in a further noise reduction. However, this means more drive lines must be used and more address decoding circuits are required.

A technique which has seen some development is that of multiple coincidence wiring. Fig. 16 shows a plane using this technique. There are four drive wires threading each core. A set of one each of X, Y, U, and V wires can be chosen so that it is completely coincident at only one core. All

other "half selected" cores on the lines are actually only quarter selected. However, there are 4 (n-1) quarter selected cores rather than 2 (n-1) half selected cores. This can result in a decrease in noise because of the more than proportionately smaller irreversible flux changes in the quarter selected cores. A variation of this technique is to let the full coincident select current be more than I_m. This results in a shorter switching time for the cores and may speed the memory cycle if noise does not become too serious.

This technique has the disadvantage of requiring considerably more complicated address decoding and drive circuits. Notice that any two drive wires uniquely determine a core. The remaining two must be selected so they are coincident at the same core. In addition, the multiple coincidence memory

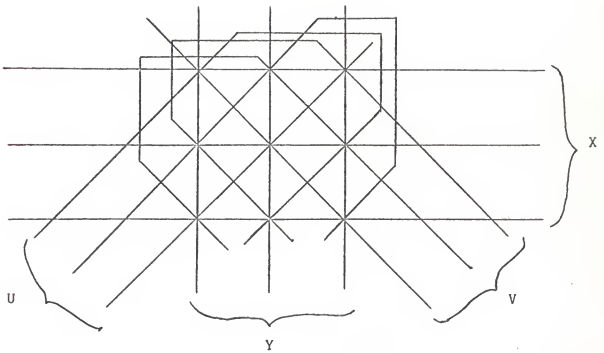

Figure 16

Multiple Coincidence Wiring.

requires a larger number of wires threading each core. This means that the core cannot be made as small and its switching time is therefore longer. For these reasons, the multiple coincidence memory has not been extensively used.

Another noise reducing scheme is the use of a deliberate post write disturb signal. Recall that a write disturbed core is always in an irreversible state with respect to reading and a read disturbed core is always in a reversible state, regardless of its major state. The post write disturb signal is a read disturbing half select signal which is deliberately generated after the write portion of the cycle so that all cores are always in a read disturbed reversible state at the completion of a cycle. This disturbing can be done either with the inhibit wire or one of the drive wires. This scheme was found by McNamara (3) to be very effective in reducing sense winding noise. However, this method is not popular because it significantly increases the memory cycle time. It is most desirable in a memory where the speed is limited by its intended use so that there is ample time for the extra signal.

A novel idea has been explored by Widrow (8). Instead of a current pulse an R.F. current is used on the two drive wires with the X current at a somewhat different frequency than the Y current. The cores are not driven hard enough to switch major states but only move along the upper or lower part of the B-H characteristic. No significant irreversible flux change takes place because of the high frequency. The slight curvature of the loop means the voltage induced in the sense winding will contain higher harmonies of the driving current frequency.

At the selected core only, a difference frequency component will also be generated. This signal can easily be selected from the noise signals of the half selected cores by filtering. Since the curvature of the B-H

characteristic is opposite in sign for the opposite major states, the phase of the difference frequency component will differ by 180° for the two states. This phase difference is used to determine the state of the selected core. Notice that this scheme is non-destructive. That is, the state of the core is not altered during reading.

Although this is a very good noise elimination scheme, in practice it is rather slow since several periods of the difference frequency are necessary to complete the memory cycle. An experimental model using this technique was able to determine the state of the addressed core after 2 μsec but required a total of 15 μsec for the system to recover and be ready for the next cycle.

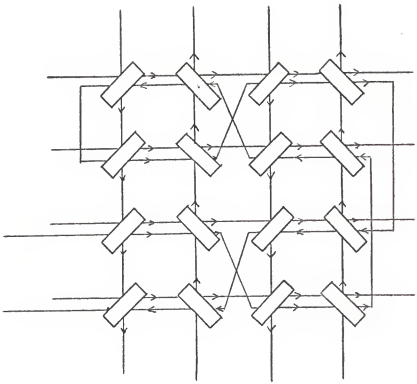

Figure 17

Rectangular Sense Winding Geometry.

The digit plane noise problem can be solved by the use of a somewhat different sense winding geometry (5). Fig. 17 shows this. The sense wire still cancels the noises produced by half selected cores. However, it also keeps all points of the wire which are equidistant from the ends close together. This means that capacitive coupling to each of these points from the Y drive wires is equal. The X drive wires are strongly capacitively coupled to the sense wire because they run parallel to it. Therefore, it is necessary to use staggered drive currents and excite the X drive wire first when this type of sense winding geometry is used.

Elder (9) has shown that a coincident current memory need not have four wires threading each core. This is of value in attempting to make the cores

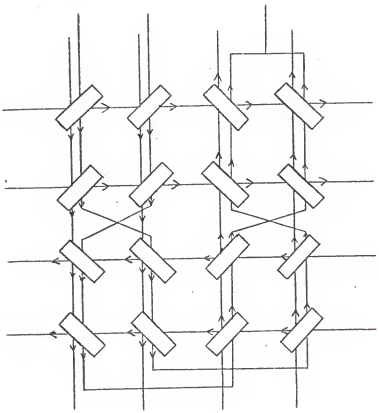

Figure 18

Combined Sense and Inhibit Wires.

themselves smaller in order to reduce their switching times. Fig. 18 shows the wiring geometry of this scheme. The sense wire is arranged so that all cores which are positively oriented with respect to it are on one section and all that are negatively oriented with respect to it are on the other section. The two sections are used in series during reading to provide for the usual noise cancellation. During writing, the two sections are used in parallel for an inhibit winding. This way, all cores are linked by inhibit current in the same direction. Thus the sense and inhibit windings are combined into one wire.

CHAPTER V

THE SWITCH CORE MATRIX

A ferrite core, because of its B-H characteristic, can be used to make a good current transformer. Consider the ϕ-I curve of Fig. 19. The saturation lines have been extended to points D and E, which have not been of interest so far. Imagine such a core used in a transformer with single turn primary and secondary windings, with the secondary connected to some sort of load. The core is initially at point A. A current pulse of magnitude greater

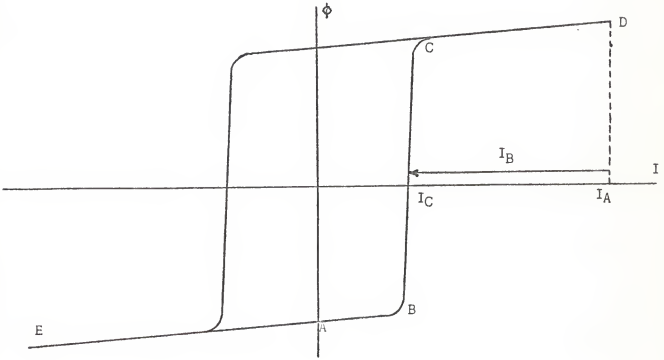

Figure 19

B-H Characteristic of a Ferrite Transformer.

than I_c is applied to the primary, with long enough rise time so that the flux changes, irreversible as well as reversible, can follow the rise. As the core moves to point B, there is little flux change and little voltage will appear at either primary or secondary terminals. However, between points B and C, the total current linking the core remains almost constant while the majority of the flux change takes place. The secondary voltage V is given by $V = -\frac{d\phi}{dt}$. Therefore, the flux change will occur at the rate necessary to induce a voltage in the secondary and therefore across its load to cause approximately $I_B = I_A - I_C$ to flow in the load. Thus for the duration of the irreversible flux change, the core makes a good current transformer. When the state of the core reaches point C, the remaining available flux change is small and the secondary current falls.

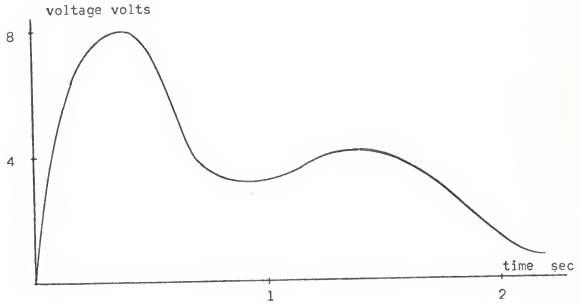

Figure 20

Voltage Developed Across a Drive Wire.

If the load is a drive wire of a storage matrix, then its voltage response to a step input of current will look like that shown in Fig. 20. Notice that this waveform is very similar to the one developed at the sense wire terminals. It arises from exactly the same factors plus wire resistance and inductance.

Now suppose such a transformer is used to drive a memory array. The transformer must be designed so that the current output pulse is of proper magnitude and duration. This can be done by adjusting the dimensions and therefore the properties of the core, and by adjusting the numbers of turns on the windings, which are not limited to one.

The primary current can be reversed near the end of the drive pulse to cause a similar reversal of the output pulse. Fig. 21 shows the output current wave form in such a case. The droop is due to the fact that the core characteristic is not perfectly vertical between points B and C in Fig. 17.

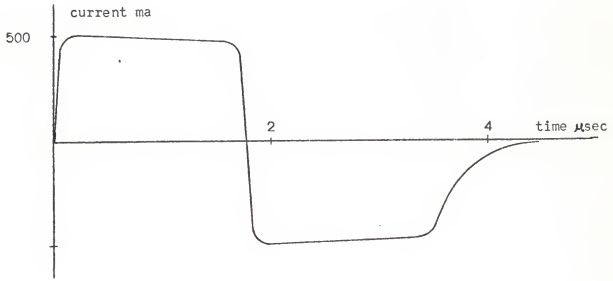

Figure 21

Current Output of a Switch Core.

The long decay after the negative pulse occurs because by this time the majority of the voltage in the load has died out and very little flux change is required to keep the current flowing. This assumes of course that the primary negative driving current has not been removed. We shall see that this often the case in practical use.

Such a transformer causes added distortion to the drive pulses and would be of no value except that it can be used in a coincident current matrix to simplify address decoding and reduce the number of driver circuits. Such a matrix is shown in Fig. 22. Each core has two half select windings,

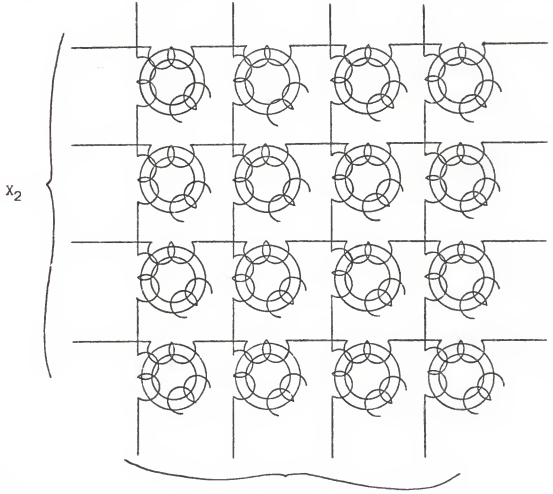

Figure 22

Switch Matrix Wiring.

an output winding, and a bias winding which is omitted for clarity. The bias windings of all cores are in series and are driven with a constant current $-\frac{I_A}{n_b}$ where n_b is the number of turns in the bias winding. This biases all cores in the matrix to point E in Fig. 19. The half select windings are wired in rows and columns like the drive wires of a memory array. The output windings are all separate and each is connected to one of the X drive wires of the memory array. A similar switch matrix is connected to the Y drive wires. This allows the X select wires to be broken down again into a coincident current selection between two sets of select wires which will be called the X_1 and X_2 wires, thus reducing the number of drive circuits from 2n to $4\sqrt{n}$ for an n x n plane.

A half-select current of $\frac{I_A}{n_s}$, where n_s is the number of turns in each select winding, supplies a total current of I_A linking the core of the intersection of the select lines. This causes a current pulse to be developed in the output winding of that core which is delivered to the corresponding X drive wire of the memory array. When the select currents are removed, the current linking the core returns to $-I_A$ and it switches back, delivering a negative drive current pulse to its associated X drive wire of the storage matrix. A half-selected switch core moves from point E to A and back to E, with negligible output. Notice that a read drive--write drive sequence has been generated at the output windings while only a single current pulse was delivered to the switch matrix. Thus, the switch matrix not only reduces the number of drive circuits necessary but makes each one simpler by requiring a current in only one direction.

Some variations of this arrangement are possible. One type supplies bias current to each row separately, removing it for the selected row. The

column is driven as before. This eliminates the bias winding and source but requires more complicated drive circuitry because separate current sources are necessary for each row. Before, only separate high current switches were needed with a common current source.

CONCLUSION

The coincident current magnetic core memory has been considered here in some detail. Its problems and limitations have been presented, and many of the techniques used to solve its problems and increase its capabilities have been discussed.

Not all of these techniques are advantageous in all situations. The requirements of a memory differ considerably with its intended use. Often speed may be sacrificed for large capacity or vice versa. Many of the techniques presented here result in such trade-offs. In more extreme cases of this nature, other types of memories may be more appropriate.

However, careful engineering, better core materials, improved array fabrication techniques, and better sense and drive circuitry have resulted in steady improvement in both speed and capacity for coincident current core memories. Early memories operated with cycles around 20 μsec in duration. Present ones are down as low as 0.5 μsec. In 1960, a memory cost \$3 to \$5 per bit (10). Presently the cost is 5¢ to 10¢ per bit. It will be interesting to see how far this development can proceed.

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COINCIDENT CURRENT MAGNETIC CORE MEMORIES

by

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B. S., Kansas State University, 1967

AN ABSTRACT OF A MASTER'S REPORT

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requirements for the degree

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Department of Electrical Engineering

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Manhattan, Kansas

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ABSTRACT

The coincident current magnetic core memory has provided immediate access storage to computers for over ten years. Unlike early drum memories, the core memory has access to any word without waiting for a mechanical motion of the magnetic medium. This report discusses the operation of this type of memory.

The ferrite magnetic core has a nearly square hysteresis loop or B-H characteristic. This means it can be left in one of two states of magnetization without any externally applied magnetic field. This properly is used to store a bit of information in a core. The nearly square B-H characteristic also means that while a particular magnetic field intensity is required to change the state of magnetization of the core, fields of half this intensity will only slightly disturb its state.

The coincident current memory uses planes involving rectangular grids of wires with the wires threading a single core at each intersection. When a current flows in one vertical and one horizontal wire, the core at the intersection is driven by a field intensity due to the sum of the currents threading it. The currents are of such magnitude that only the core of the intersection of the wires changes state.

The previous state of the core is determined by the voltage induced on sense wires, one of which threads every core in each plane. A separate plane is present for each bit of a word. Writing is accomplished by reversing the currents in the horizontal and vertical wires. In planes where the selected core's state is not to be changed, a current flows in a fourth wire called

the inhibit wire which threads every core in the plane. This current links the core in a direction opposite from that of the other currents, so that the applied field is insufficient to switch the core.

Disturbed cores also induce small noise voltages on the sense wire. Because of the large number of disturbed cores, the sum of these voltages presents a serious problem. The sense wire is therefore arranged so the individual noise voltages tend to cancel, although complete cancellation is not possible. Many additional techniques have been used to combat the noise problem.

A coincident current matrix of cores is also often used to further simplify address decoding. This matrix uses cores as current transformers and selects them from a rectangular array in the same way that memory cores are selected in a plane.

Coincident current core memories have been the most successful type and have seen immense improvements in the past ten years.